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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/634,278	GUY ET AL.	
	Examiner	Art Unit	
	Victor W. Wang	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) *14-19,33-39 and 55-62* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,20-32 and 40-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12 November 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10634278 has a total of 62 claims pending in the application; there are 3 independent claim, 38 dependent claims and 21 withdrawn claims.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The application's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. ELECTION/RESTRICTIONS

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-13, 20-32, and 40-54, drawn to a method for virtual to physical memory translation, classified in class 711, subclass 4.

II. Claims 14-19, 33-39, and 55-62, drawn to a method for sharing a resource between multiple users using virtual devices, classified in class 718, subclass 1.

4. Inventions Group I and Group II are related as subcombinations disclosed as usable together in a single combination. Group I is drawn to a method for virtual to physical memory translation. Group II is drawn to a method for sharing a resource between multiple users using virtual devices. The subcombinations are distinct if they do not overlap in scope and are not

obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, inventions Group I and Group II have a separate utility and the search for the Group I invention is not required for the Group II invention and vice versa. See MPEP § 806.05(d).

5. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

7. During a telephone conversation with Mark A. Goldstein, Reg. No. 50,759 on 04/26/2007 a provisional election was made without traverse to prosecute the invention of Group I, claim 1-13, 20-32, and 40-54. Affirmation of this election must be made by applicant in replying to this Office action. Claims 14-19, 33-39, and 55-62 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

8. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

III. INFORMATION CONCERNING INFORMATION DISCLOSURE STATEMENT

Information Disclosure Statement

9. The information disclosure statement (IDS) filed 12 November 2003, with the exception of disclosed NPL documents titled "PowerQuest, Partitioning White Paper for PartitionMagic" and "PowerQuest product description for Partition Magic 8.0", is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement, with the exception of the aforementioned NPL documents, is being considered by the examiner. NPL documents titled "PowerQuest, Partitioning White Paper for PartitionMagic" and "PowerQuest product description for Partition Magic 8.0" fail to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the document does not contain a date of publication including at least the month and year of publication. Said NPL document has been placed in the application file, but the has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

IV. INFORMATION CONCERNING DRAWINGS

Drawings

10. The drawings received 5 August 2003 is in compliance with the provisions of 37 CFR 1.84(p)(5). Accordingly, the drawings are being considered by the examiner.

V. REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. **Claims 9, 25, 28, and 48** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 9, 28 and 48 recites the limitation "wherein the subtracting comprises: referring to a virtual device table." The limitation is considered to be indefinite and unclear because it is not apparent to the examiner how the action of adding or subtracting from a virtual address is associated with virtual device table. It is not clear how the virtual device table is referenced in adding or subtracting from a virtual address.

Claim 25 recites the limitation "wherein the adding comprises: referring to a virtual device table". The limitation is considered to be indefinite and unclear because it is not apparent to the examiner how the action of adding or subtracting from a virtual address is associated with virtual device table. It is not clear how the virtual device table is referenced in adding or subtracting from a virtual address.

VI. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. **Claims 1, 4-5, 10, 20, 22-23, 29, 40, 43-44, 49, 53-54** are rejected under 35 U.S.C. 102(b) as being anticipated by Fukunaga (US 4481573).

As per claims 1, 20 and 40, Fukunaga discloses "receiving a hard disk access command including a virtual hard disk address translating the virtual hard disk address to a translated address forwarding to the hard disk the access command with the translated address in place of the hard disk address." **[With respect to this limitation, Fukunaga discloses "a main memory and an external memory are regarded to be apparently integral" (column 1, lines 25-26), and "a virtual address of the instruction word is transferred to the memory control unit 12 through the common bus 50. The money control unit 12 translates the virtual address to the physical address to access the main memory 10 through the memory bus11." (column 6, lines 48-54), "A data processing system in which a main memory is shared by a plurality of processors is generally called a multiprocessor system " (column 1, lines 18-20) and Fig. 1. The examiner notes the differences between claims 1 and 20, and draws reference between the "virtual address" as disclosed by Fukunaga to applicant's "virtual hard disk address" in claim 1, and "hard disk address" in claim 2.]**

As per claims 4, 22 and 43, Fukunaga discloses "mapping the virtual hard disk address to a real hard disk address." **[With respect to this limitation, Fukunaga discloses "An address for the memory access by the processor is given by a virtual address, a high order address field of which is used to look up the translation table to effect the translation to the physical address. Since as many such translation tables as the number of pages of the virtual addresses are required" (column 1, lines 46-51), where the "active virtual device address" of claim 22 is equivalent to "virtual hard disk address" of claim 4, and "hard disk address" of claim 22 is equivalent to "real hard disk address" of claim 4. The equivalence is draw for the rest of the office action.]**

As per claims 5, 23 and 44, Fukunaga discloses "referring to a virtual device table." **[With respect to this limitation, Fukunaga discloses "An address for the memory access by the processor is given by a virtual address, a high order address field of which is used to look up the translation table to effect the translation to the physical address. Since as many such translation tables as the number of pages of the virtual addresses are required" (column 1, lines 46-51)]**

As per claims 10, 29 and 49, Fukunaga discloses "wherein the sharing device is one of a field programmable gate array (FPGA), a programmable logic unit (PLU), an application specific integrated circuit (ASIC)." **[With respect to this limitation, Fukunaga discloses Fig. 11, where it is understood that reference number 12 is the memory control unit responsible for memory access between processors, and the memory control comprises of an ALU and other circuitry which makes it an ASIC.]**

As per claim 53, Fukunaga discloses "The method of claim 40 wherein the sharing device is included in the storage device." **[With respect to this limitation, Fukunaga discloses "Fig. 9 shows a configuration of the MCU" (column 4, line 47), which contains both the memory control unit (sharing device) and the main memory.]**

As per claim 54, Fukunaga discloses "The method of claim 40 wherein the storage device is a hard disk drive." **[With respect to this limitation, Fukunaga discloses "a main memory and an external memory are regarded to be apparently integral" (column 1, lines 25-26)]**

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. **Claims 2, 7, 21, 26, 41, 46** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukunaga (US 4481573) in view of Aguilar (US 6799316).

As per claims 2, 21 and 41, Fukunaga discloses "receiving a response to the access command... forwarding the response" **[With respect to this limitation, Fukunaga discloses "the read data 154 is transferred to the data bus 56 through a bus 155, and an end signal and the return code (RC) are transferred to the response bus 57 through a bus 156 to send them back to the requesting processor" (column 9, lines 37-40)];** but fails to disclose expressly "receiving a response to the access command from the hard disk if the response

includes a hard disk address, translating the hard disk address into a virtual disk address forwarding the response with the virtual disk address in place of the hard disk address."

Aguilar discloses "receiving a response to the access command from the hard disk if the response includes a hard disk address, translating the hard disk address into a virtual disk address forwarding the response with the virtual disk address in place of the hard disk address." **[With respect to this limitation, Aguilar discloses "the SMI trap receiving a signal on the address bus (step 502). Addresses are sent over the address bus to signal a memory location that data will follow. A physical memory address associated with the signal is then determined (step 504).... Each time a memory address appears on the address bus the SMI trap compares the address with a list of memory addresses corresponding to virtual hardware devices (step 506).... If, on the other hand, the memory address being transmitted on the address bus does match a virtual hardware device... both the address and the IO instruction and/or the IO instruction type (read, write etc.) are stored (step 510). Finally, the SMI trap generates a system management interrupt (SMI) message.... Alternatively, the SMI message may include both the identity of the SMI trap and information received by the SMI trap such as the memory address and IO instruction. The process then ends." (column 7-8, lines 62-21)]**

Fukunaga and Aguilar are analogous art because they are from the same field of endeavor of data transfer process methods.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the data transfer process method that contains a device that receives a virtual address, translate the virtual address, and sends the translated address as described by Fukunaga

and determine to receive a response by the device which contains a translated address, translate the translated address back into virtual address as taught by Aguilar.

The motivation would have been because Aguilar teaches that **"the present invention provides a convenient means for replacing faulty or out-of-date hardware components with virtual hardware devices." (column 8, lines 25-27)**

Therefore, it would have been obvious to combine Aguilar and Fukunaga for the benefit of convenience as specified in claims 2, 21 and 41.

As per claims 7, 26 and 46, Fukunaga discloses "wherein the translating the hard disk address comprises: mapping the response address to the virtual address by referring to a virtual device table." **[With respect to this limitation, Fukunaga discloses "An address for the memory access by the processor is given by a virtual address, a high order address field of which is used to look up the translation table to effect the translation to the physical address. Since as many such translation tables as the number of pages of the virtual addresses are required" (column 1, lines 46-51), where it is understood that "the hard disk address" of claim 7 is equivalent to the "response address" of claim 26]**

17. **Claims 3 and 42** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukunaga (US 4481573) in view of Aguilar (US 6799316) and Hsu (US 5526504).

As per claims 3 and 42, Fukunaga fails to disclose expressly "if the response includes a hard disk size, translating the hard disk size into a virtual disk size forwarding the response with the virtual disk size in place of the hard disk size."

Aguilar discloses "if the response includes a hard disk size, translating the hard disk size into a virtual disk size forwarding the response with the virtual disk size in place of the hard disk size." **[With respect to this limitation, Aguilar discloses "the SMI trap receiving a signal on the address bus (step 502). Addresses are sent over the address bus to signal a memory location that data will follow. A physical memory address associated with the signal is then determined (step 504).... Each time a memory address appears on the address bus the SMI trap compares the address with a list of memory addresses corresponding to virtual hardware devices (step 506).... If, on the other hand, the memory address being transmitted on the address bus does match a virtual hardware device... both the address and the IO instruction and/or the IO instruction type (read, write etc.) are stored (step 510). Finally, the SMI trap generates a system management interrupt (SMI) message.... Alternatively, the SMI message may include both the identity of the SMI trap and information received by the SMI trap such as the memory address and IO instruction. The process then ends." (column 7-8, lines 62-21)].**

Fukunaga, Aguilar and Hsu are analogous art because they are from the same field of endeavor of data transfer process methods.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the data transfer process method that contains a device that receives a virtual address, translate the virtual address, and sends the translated address as described by Fukunaga and determine to receive a response by the device which contains a translated address, translate the translated address back into virtual address as taught by Aguilar.

The motivation for doing so would have been because Aguilar teaches that **"the present invention provides a convenient means for replacing faulty or out-of-date hardware components with virtual hardware devices." (column 8, lines 25-27)**

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the data transfer process method that contains a device that receives a virtual address, translate the virtual address, and sends the translated address as described by Fukunaga, determine to receive a response by the device which contains a translated address, translate the translated address back into virtual address as described by Aguilar and determine to send size information as well as address information as taught by Hsu.

Although Aguilar teaches sending a physical address to a translation unit, translate the address into virtual address, it does not clearly and specifically disclose that the physical address may include a size. Hsu discloses "a hard disk size" and "virtual disk size" **[With respect to this limitation, Hsu discloses "Page address output circuit 112 outputs virtual and physical page addresses over communication paths 152 and 156, respectively, and outputs a match signal over a communication path 160. Page address output circuit 112 receives the... addresses to be translated over a communication path 164, receives a global and page size signal over a communication path 168." (column 6, lines 15-21), where it is understood that while Aguilar discloses translating physical to virtual address, Hsu discloses that size signal are sent and received with the virtual addresses].** The motivation for doing so would have been because Hsu teaches that **"it is advantageous to have a TLB that can support multiple page sizes, allowing certain high-end applications to work with large pages and other applications to work with smaller pages." (column 2, lines 27-31)**

Therefore, it would have been obvious to combine Hsu with Fukunaga and Aguilar for the benefit of supporting multiple page sizes as specified in claims 3 and 42.

18. **Claims 8-9, 27-28, 47-48** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukunaga (US 4481573) in view of Aguilar (US 6799316) and Porterfield (US 6799316)

As per claims 8, 27 and 47, Fukunaga and Aguilar fails to disclose expressly "wherein the translating the hard disk address comprises: subtracting an offset from the response address based on identifying information of an active virtual device."

Porterfield discloses "wherein the translating the hard disk address comprises: subtracting an offset from the response address based on identifying information of an active virtual device." **[With respect to this limitation, Porterfield discloses "virtual addresses often include a page number and an offset" (column 2, lines 40-41), Fig. 5a, where "FIG. 5a is a diagram illustrating the translation of a virtual address to a physical address of one embodiment of the present invention." (column 5, lines 44-46), where it is understood that an offset is subtracted from virtual address. It is further understood that the offset from each virtual address is subtracted or added once the specific virtual address is accessed. "hard disk address" of claim 8 is equivalent to "response address" of claim 27]**

Fukunaga, Aguilar and Porterfield are analogous art because they are from the same field of endeavor of data transfer process methods.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the data transfer process method that contains a device that receives a virtual address, translate the virtual address, and sends the translated address as described by Fukunaga,

determine to receive a response by the device which contains a translated address, translate the translated address back into virtual address as described by Aguilar and determine that the translating processes includes subtracting an offset to the virtual address based upon mapping information as taught by Porterfield.

The motivation would have been Porterfield teaches that **"the architecture of the present invention reduces the total system cost" (column 6, lines 23-24)**

Therefore, it would have been obvious to combine Porterfield with Fukunaga and Aguilar for the benefit of reducing total system cost as specified in claims 8, 27 and 47.

As per claims 9, 28 and 48 Fukunaga fails to disclose expressly "wherein the subtracting comprises: referring to a virtual device table."

Porterfield discloses "wherein the subtracting comprises: referring to: a virtual device table." **[With respect to this limitation, Porterfield discloses "virtual addresses often include a page number and an offset.... In order to translate between the virtual and physical addresses, a basic virtual memory system creates a series of lookup tables, called page tables.... These page tables store the virtual address pages numbers used by the computer. Stored with each virtual address page number is the corresponding physical address page number" (column 2, lines 40-48), Fig. 5a, where "FIG. 5a is a diagram illustrating the translation of a virtual address to a physical address of one embodiment of the present invention." (column 5, lines 44-46), where it is understood that an offset is subtracted from virtual address. It is further understood that the offset from each virtual address is subtracted or added once the specific virtual address is accessed]**

Fukunaga, Aguilar and Porterfield are analogous art because they are from the same field of endeavor of data transfer process methods.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the data transfer process method that contains a device that receives a virtual address, translate the virtual address, and sends the translated address as described by Fukunaga, determine to receive a response by the device which contains a translated address, translate the translated address back into virtual address as described by Aguilar and determine that the translating processes includes subtracting an offset to the virtual address based upon mapping information in a table as taught by Porterfield.

The motivation would have been Porterfield teaches that **"the architecture of the present invention reduces the total system cost" (column 6, lines 23-24)**

Therefore, it would have been obvious to combine Porterfield with Fukunaga and Aguilar for the benefit of reducing total system cost as specified in claims 9, 28 and 48.

19. **Claims 6, 11-13, 24-25, 30-32, 45, 50-52** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukunaga (US 4481573) in view of Porterfield (US 6799316).

As per claims 6, 24 and 45, Fukunaga fails to disclose "wherein the translating comprises: adding an offset to the virtual hard disk address based on virtual device identifying information stored in a virtual device table."

Porterfield discloses "wherein the translating comprises: adding an offset to the virtual hard disk address based on virtual device identifying information stored in a virtual device table." **[With respect to this limitation, Porterfield discloses "virtual addresses often include**

a page number and an offset" (column 2, lines 40-41), Fig. 5a, where "FIG. 5a is a diagram illustrating the translation of a virtual address to a physical address of one embodiment of the present invention." (column 5, lines 44-46), where it is understood that virtual address is combined with an offset to translate.]

Fukunaga, and Porterfield are analogous art because they are from the same field of endeavor of data transfer process methods.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the data transfer process method that contains a device that receives a virtual address, translate the virtual address, and sends the translated address as described by Fukunaga and determine that the translating processes includes adding an offset to the virtual address based upon mapping information as taught by Porterfield.

The motivation would have been Porterfield teaches that **"the architecture of the present invention reduces the total system cost" (column 6, lines 23-24)**

Therefore, it would have been obvious to combine Porterfield and Fukunaga for the benefit of reducing total system cost as specified in claims 6, 24 and 45.

As per claim 25, Fukunaga discloses "wherein the adding comprises: referring to a virtual device table." **[With respect to this limitation, Fukunaga discloses "An address for the memory access by the processor is given by a virtual address, a high order address field of which is used to look up the translation table to effect the translation to the physical address. Since as many such translation tables as the number of pages of the virtual addresses are required" (column 1, lines 46-51)]**

As per claims 11, 30 and 50, Fukunaga fails to disclose expressly "wherein the sharing device is coupled between the hard disk and a motherboard of the computer."

Porterfield discloses "wherein the sharing device is coupled between the hard disk and a motherboard of the computer." **[With respect to this limitation, Porterfield discloses "This graphics processor can be described by reference to FIG. 2, which illustrates a graphics/memory control unit 120 including a graphics processor unit 122 that communicates with a memory control unit 124." (column 4, lines 1-4), "Peripherals 114 and the graphics accelerator 110 communicate with main memory 106 and system logic 104 through the system bus 108. The standard system us 108 is currently the Peripherals Connection Interface (PCI).... PCI supports multiple peripheral components and add-in cards.... Three dimensional (3D) graphics applications, threatens to overload the PCI bus." (column 1, lines 37-52), where it is understood that the motherboard is an integral component of any computer. It is further understood that the memory control unit (sharing device) is placed on a separate graphics add-in card which also contains graphics processor, and communicates with a main memory thru a PCI bus, and these components are all placed on the motherboard.]**

Fukunaga, and Porterfield are analogous art because they are from the same field of endeavor of data transfer process methods.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the data transfer process method that contains a device that receives a virtual address, translate the virtual address, and sends the translated address as described by Fukunaga

and determine that the device is coupled on a graphics card coupled to both a motherboard and a main memory as taught by Porterfield.

The motivation would have been Porterfield teaches that **"the architecture of the present invention reduces the total system cost" (column 6, lines 23-24)**

Therefore, it would have been obvious to combine Porterfield and Fukunaga for the benefit of reducing total system cost as specified in claims 11, 30 and 50.

As per claims 12, 31 and 51, Fukunaga fails to disclose expressly "wherein the sharing device is coupled to a motherboard included in the computer."

Porterfield discloses "wherein the sharing device is coupled between the hard disk and a motherboard of the computer." **[With respect to this limitation, Porterfield discloses "This graphics processor can be described by reference to FIG. 2, which illustrates a graphics/memory control unit 120 including a graphics processor unit 122 that communicates with a memory control unit 124." (column 4, lines 1-4), "Peripherals 114 and the graphics accelerator 110 communicate with main memory 106 and system logic 104 through the system bus 108. The standard system us 108 is currently the Peripherals Connection Interface (PCI).... PCI supports multiple peripheral components and add-in cards.... Three dimensional (3D) graphics applications, threatens to overload the PCI bus." (column 1, lines 37-52), where it is understood that the motherboard is an integral component of any computer. It is further understood that the memory control unit (sharing device) is placed on a separate graphics add-in card which also contains graphics**

processor, and communicates with a main memory thru a PCI bus, and these components are all placed on the motherboard.]

Fukunaga, and Porterfield are analogous art because they are from the same field of endeavor of data transfer process methods.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the data transfer process method that contains a device that receives a virtual address, translate the virtual address, and sends the translated address as described by Fukunaga and determine that the device is coupled on a graphics card coupled to both a motherboard and a main memory as taught by Porterfield.

The motivation would have been Porterfield teaches that **"the architecture of the present invention reduces the total system cost" (column 6, lines 23-24)**

Therefore, it would have been obvious to combine Porterfield and Fukunaga for the benefit of reducing total system cost as specified in claims 12, 31 and 51.

As per claims 13, 32 and 52, Fukunaga fails to disclose expressly "wherein the sharing device is included on a card to be coupled to a card slot in the computer."

Porterfield discloses "wherein the sharing device is coupled between the hard disk and a motherboard of the computer." **[With respect to this limitation, Porterfield discloses "This graphics processor can be described by reference to FIG. 2, which illustrates a graphics/memory control unit 120 including a graphics processor unit 122 that communicates with a memory control unit 124." (column 4, lines 1-4), "Peripherals 114 and the graphics accelerator 110 communicate with main memory 106 and system logic 104**

through the system bus 108. The standard system us 108 is currently the Peripherals Connection Interface (PCI).... PCI supports multiple peripheral components and add-in cards.... Three dimensional (3D) graphics applications, threatens to overload the PCI bus." (column 1, lines 37-52), where it is understood that the motherboard is an integral component of any computer. It is further understood that the memory control unit (sharing device) is placed on a separate graphics add-in card which also contains graphics processor, and communicates with a main memory thru a PCI bus, and these components are all placed on the motherboard.]

Fukunaga, and Porterfield are analogous art because they are from the same field of endeavor of data transfer process methods.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the data transfer process method that contains a device that receives a virtual address, translate the virtual address, and sends the translated address as described by Fukunaga and determine that the device is coupled on a graphics card coupled to both a motherboard and a main memory as taught by Porterfield.

The motivation would have been Porterfield teaches that **"the architecture of the present invention reduces the total system cost" (column 6, lines 23-24)**

Therefore, it would have been obvious to combine Porterfield and Fukunaga for the benefit of reducing total system cost as specified in claims 13, 32 and 52.

VII. RELEVANT ART CITED BY THE EXAMINER

20. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**

The following reference teaches data transfer control methods.

U.S. PATENT NUMBER

US 6006322

U.S. PATENT PUBLICATION NUMBER

US 2002/0049871

US 2003/0018875

Conclusion

21. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor W. Wang whose telephone number is (571) 272-9771. The examiner can normally be reached on Monday through Friday, 8:30am - 6:00pm. E.S.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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8 May, 2007

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